



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
1875.1390002APPLICATION NO.
10/700,443FIRST NAMED INVENTOR
Janardhanan S. AJITFILING DATE
November 5, 2003ART UNIT
2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
<i>WTA</i>	AA1	2001/0026178 A1	10/2001	Itoh <i>et al.</i>			
<i>WTA</i>	AB1	5,719,509	02/1998	Chan			
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<i>WTA</i>	AD1	6,060,907	05/2000	Vishwanthaiah <i>et al.</i>			
<i>WTA</i>	AE1	6,137,322	10/2000	Ten Eyck			
<i>WTA</i>	AF1	6,144,218	11/2000	Smith <i>et al.</i>			
<i>WTA</i>	AG1	6,177,819 B1	01/2001	Nguyen			
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
<i>WTA</i>	AK1	DE 40 18 754 A1	12/1991	DE			N
	AL						Yes No
	AM						Y S N
	AN						Y S No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

<i>WTA</i>	AO	1	European Search Report from European Patent Application No. 03250012.6, 4 pages, mailed March 26, 2003.
<i>WTA</i>	AP	1	Choy, C.S. <i>et al.</i> , "A Low Power-Noise Output Driver with an Adaptive Characteristic Applicable to a Wide Range of Loading Conditions," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 32, No. 6, pp. 913-917 (June 1997).
<i>WTA</i>	AQ	1	Huchzermeier, J., "Saubere und schnelle schalten Dynamic Output Control ermöglicht verbesserte Schalteigenschaften bei hohen Geschwindigkeiten," <i>Elektronik</i> , Vol. 48, N. 20, pp. 50-54, 56 and 58 (October 5, 1999).
<i>WTA</i>	AR	1	CMOS Integrated Circuits, B-Series, Solid State Scientific, Inc., pp. 16-17 (November 1976).

EXAMINER

DATE CONSIDERED

4/29/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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SKGF Rev. 12/03/03